

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)			ATTY. DKT. NO. 5681-03600 APPLICANT: Frankel, et al. FILING DATE: November 9, 2001	SERIAL NO. 10/007,816 GROUP: 2151			
U.S. PATENT DOCUMENTS							
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	5,812,824	9/22/98	Dearth, et al.			
	A2	5,732,247	3/24/98	Dearth, et al.			
	A3	5,881,267	3/9/99	Dearth, et al.			
	A4	5,848,236	12/8/98	Dearth, et al.			
	A5	6,031,987	2/29/00	Damani, et al.			
	A6	5,910,903	6/8/99	Feinberg, et al.			
	A7	5,850,345	12/15/98	Son			
	A8	6,053,947	4/25/00	Parson			
	A9	5,870,585	2/9/99	Stapleton			
	A10	5,751,941	5/12/98	Hinds, et al.			
	A11	5,634,010	5/27/97	Ciscon, et al.			
	A12	6,117,181	9/12/00	Dearth, et al.			
	A13	5,519,848	5/21/96	Wloka, et al.			
	A14	5,442,772	8/15/95	Childs, et al.			MAR 01 2002
	A15	5,339,435	8/19/94	Lukin, et al.			Technology Center 2100
	A16	4,456,994	6/26/84	Segarra			
	A17	5,625,580	4/29/97	Read, et al.			
	A18	5,715,184	2/3/98	Tyler, et al.			
	A19	5,794,005	8/11/98	Steinman			
	A20	5,907,695	5/25/99	Dearth			
	A21	4,821,173	4/11/89	Young, et al.			
	A22	4,937,173	6/26/90	Kanda, et al.			
	A23	5,185,865	2/9/93	Pugh			
	A24	5,327,361	7/5/94	Long, et al.			
	A25	5,455,928	10/3/95	Herlitz			
	A26	6,345,242	2/5/02	Dearth, et al.			

EXAMINER:

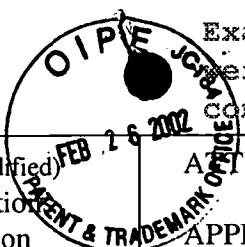
/David Silver/ (01/15/2009)

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Information Disclosure Statement--PTO 1449 (modified)

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Examiner Note: The crossed out reference
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
A28	"Rule Base Driven Conversion of an Object Oriented Design Structure Into Standard Hardware Description Languages." Verschueren, A.C., IEEE Xplore, appears in Euromicro Conference, 1998, Proceedings, 24 th , vol. 1, August 25, 1998, pages 42-45.		
A29	"Modeling Communication with Objective VHDL," Putzke, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings, 1998 International, March 16, 1998, pages 83-89.		
A30	"A Procedural Language Interface for VHDL and its Typical Applications," Martinolle, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings, 1998 International, March 16, 1998, pages 32-38.		
A31	"The Verilog Procedural Interface for the Verilog Hardware Description Language," Dawson, et al., IEEE Xplore, appears in Verilog HDL Conference, 1996, Proceedings, 1996 International, February 26, 1996, pages 17-23.		
A32	"An Integrated Environment for HDL Verification," York, et al., IEEE Xplore, appears in Verilog HDL Conference, 1995, Proceedings, 1995 International, March 27, 1995, pages 9-18.		
A33	"The PowerPC 603 C++ Verilog Interface Model," Voith, R.P., IEEE Xplore, appears in Compcon Spring '94, Digest of Papers, Feb. 28, 1994, pages 337-340.		
A34	"Networked Object Oriented Verification with C++ and Verilog," Dearth, et al., IEEE, XP-002144328, 1998, 4 pages.		
A35	Patent Abstracts of Japan, publication no. 10326835, published December 8, 1998.		
A36	Patent Abstracts of Japan, publication no. 10049560, published February 20, 1998.		
A37	Patent Abstracts of Japan, publication no. 10340283, published December 22, 1998.		
A38	Patent Abstracts of Japan, publication no. 07254008, published October 3, 1995.		
A39	"Multiprocessing Verilog Simulator Exploits the Parallel Nature of HDLs." Lisa Maliniak, Electronic Design, Abstract, May 30, 1994, 1 page.		
A40	"It's A Multithreaded World, Part 1," Charles J. Northrup, BYTE, May 1992, 7 pages.		
A41	"It's a Multithreaded World, Part 2," Charles J. Northrup, BYTE, June 1992, pp. 351-356.		
A42	"Weaving a Thread," Sheki Press, BYTE, October 1995, pp. 173-174.		
A43	"Making Sense of Collaborative Computing," Mark Gibbs, Network World Collaboration, January 10, 1994, 4 pages.		
A44	"Parallel Logic Simulation of VLSI Systems," Bailey, et al., ACM Computing Surveys, Vol. 26, No. 3, September 1994, pp. 255-294.		
A45	"Multithreaded Languages for Scientific and Technical Computing," Cherri M. Pancake, Proceedings of the IEEE, Vol. 81, No. 2, February 1993, pp. 288-304.		
A46	"Distributed Simulation Architecture, SW Environment, Enterprise Server Products," Purdue EE400 Presentation by Freyensee and Frankel, November 9, 2000, 13 pages.		

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
A47	"BNF and EBNF: What Are They And How Do They Work?," Lars Marius Garshol, October 12, 1999, pp. 1-10.		
A48	"VCK: Verilog-C Kernel," Testbench Automation, Distributed by Verilog Simulation, Hardware-Software Co-verification, 2001 Avery Design Systems, Inc., 8 pages.		
A49	"Principles of Verilog-PLI," Swapna Jit Mitra, Silicon Graphics Incorporated, 1999, 10 pages.		
A50	"IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language," IEEE, December 12, 1995, 8 pages.		
A51	"OpenVera 1.0, Language Reference Manual," Version 1.0, March 2001, pp. 4-1 to 4-34, pp. 5-1 to 5-32, 6-1 to 6-22, 7-1 to 7-24, 11-1 to 11-50, 12-1 to 12-8, 13-1 to 13-14, 14-1 to 14-20, 15-1 to 15-118.		
A52	"VLSI Design of a Bust Arbitration Module for the 68000 Series of Microprocessors," Ososanya, et al., IEEE, 1994, pp. 398-402.		
A53	"A VHDL Standard Package for Logic Modeling," David R. Coelho, IEEE Design & Test of Computers, Vol. 7, Issue 3, June 1990, pp. 25-32		
A54	"Corrected Settling Time of the Distributed Parallel Arbiter," M.M. Taub, PhD., IEEE Proceedings, Part E: Computers & Digital, Vol. 139, Issue 4, July 1992, pp. 348-354.		
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